

A novel structure designed for high density nonvolatile memory devices

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Abstract—The same as in microprocessor fabrication, non-volatile memory devices are facing the problem in device size scaling down, such as large leakage current density. High-k materials are considered to solve it. However, simply replacing low-k to high-k materials, while keeping the structure as before, is not a good solution. Based on our analysis, we proposed a novel structure, in which charges are injected from top gate electrode. In this structure, high charge injection, large memory window and long retention time can be expected.

Index Terms—charge injection from top gate electrode, non-volatile memory, high-k dielectric, device efficiency

I. INTRODUCTION

NONVOLATILE memory (NVM) has attracted great interests for its enormous applications since its invention. [1] Large volume, high speed NVM devices are highly demanded in many fields, such as portable memory sticks, smart phones, digital cameras, etc. To achieve large volume and high speed, the size of device approaches to the physical limit. [2] The capacitance of single devices thus needs to be large enough to maintain channel current large enough to keep a high on-off ratio. If the traditional gate dielectric material, SiO_2 , is used, it urges the thickness of the dielectric gate to a unprecedented thin level (around or below 1nm). Thus high-k materials are proposed to replace SiO_2 , which has been utilized in microprocessor fabrication. [3] In NVM, the common way to use high-k materials is simply change SiO_2 to high-k materials. [4], [5] However, we found that in this way, the performance is compromised in traditional floating gate NVM device structure. In this Letter, we proposed a novel NVM structure, in which the charges are injected from top gate electrode. By this way, it is possible to achieve scaling down further without performance compromise.

II. A CONTRADICTION IN TRADITIONAL FLOATING GATE NVM

In traditional NVM devices, the charges are injected from substrate/source, as shown in Fig. 1(a) (Model 1). Insulator 2 acts as a potential barrier in charge injection, for which lower barrier and thinner thickness will benefit the injection efficiency. However, in this structure, insulator 2 also acts as gate dielectric. For this function, the insulation of insulator 2 is crucial for the device performance, which demands higher barrier and thicker thickness. From above statement, we can find that there exists a conflicting requirement for insulator 2. This arises from the dual functions of insulator 2. This conflict becomes severe as the device size approaches the physical limit. [2]

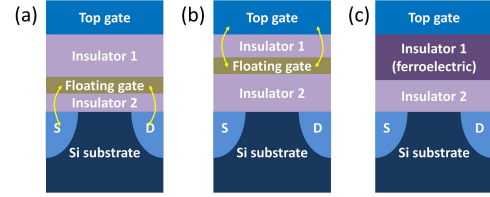


Fig. 1: (a) Model 1. Floating gate NVM structure with charge injection from substrate or source. (b) Model 2. Floating gate NVM structure with charge injection from top gate electrode. (c) Ferroelectric NVM structure.

To overcome this difficulty, we propose a novel structure, in which the charges are injected from top gate electrode, as shown in Fig. 1(b) (Model 2). The insulator 1 acts as tunneling potential barrier and insulator 2 acts as gate dielectric. In this structure, each insulator layer plays one single function, thus they can be optimized respectively.

III. STRUCTURE AND FORMULAE

A typical structure of floating gate NVM devices is shown in Fig. 2(a). The equivalent electronic circuit is depicted in Fig. 2(b). Each insulator layer is characterized by one capacitor. The capacitance between insulator 1 and the substrate is characterized by a variable capacitor depending on the interface state. The floating gate is represented by stored charge Q_{fg} . The band bending is neglected for simplicity when V and Q_{fg} are zeros.

For usable memory devices, the leakage is generally in low levels. For theoretical analysis, we assume the resistance of the structure is large enough to be ignored, while in real cases it should be critically addressed.

According to Kirchhoff's voltage law, we obtain Equ. 1.

$$V_1 + V_2 + V_3 = V \quad (1)$$

where V_1 , V_2 and V_3 are the voltage applied on C_1 , C_2 and C_3 , respectively. V is the total voltage. According to charge

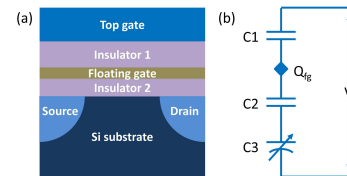


Fig. 2: (a) Layer structure of a typical NVM device. (b) Schematic diagram of the electronic circuit to model the device structure of (a).

conservation, we obtain Eqs. (2) and (3).

$$V_2 C_2 = V_1 C_1 + Q_{fg} \quad (2)$$

$$V_2 C_2 = V_3 C_3 \quad (3)$$

By combining Eqs. (1)-(3), the voltages applied on each layer and the interface between insulator 2 and substrate can be resolved, as shown in Eqs. (4)-(6).

$$V_1 = \frac{V C_2 C_3 - Q_{fg}(C_2 + C_3)}{C_1 C_2 + C_2 C_3 + C_3 C_1} \quad (4)$$

$$V_2 = \frac{(V C_1 + Q_{fg}) C_3}{C_1 C_2 + C_2 C_3 + C_3 C_1} \quad (5)$$

$$V_3 = \frac{(V C_1 + Q_{fg}) C_2}{C_1 C_2 + C_2 C_3 + C_3 C_1} \quad (6)$$

The following analysis is based on the Eqs. (4)-(6), to discuss how to optimize memory window, electric field on the two insulator layers, and the influence of stored charges.

IV. OPTIMIZATION CONDITIONS

In this section, we discuss the requirements on optimizing the structure. Three aspects are discussed, which are essential for NVM performance. They are memory window, charge injection efficiency and the effect of stored charges.

A. Memory window

The memory window can be defined by the flat band voltage shift due to charge storage. For NVM structure, flat band means the band diagram of insulator 2 is flat, i.e. $V_2 = 0$. From Equ. (5), by combining $V_2 = 0$, we obtain $V = -\frac{Q_{fg}}{C_1}$. In general, we assume positive and negative charges can all be stored in floating gate. Then the memory window can be expressed as follows,

$$V_{window} = \frac{|Q_1| + |Q_2|}{C_1} \quad (7)$$

where Q_1 and Q_2 are the stored charge in the floating gate by positive and negative charge injection, respectively. From Equ. (7), V_{window} is proportional to $\frac{1}{C_1}$. Thus, the memory window can be tuned by the capacitance of insulator 1. Generally, for a large memory window, small C_1 is needed.

B. Charge injection efficiency

The efficiency of charge injection is dependent on the electric field applied on tunneling barrier (insulator 1 or insulator 2) in F-N tunneling mechanism. [6] To elucidate the tunneling efficiency, from Eqs. (4) and (5), we deduced Equ. (8).

$$\frac{\partial E_1}{\partial V} / \frac{\partial E_2}{\partial V} = \frac{\partial V_1}{\partial V} / \frac{\partial V_2}{\partial V} = \frac{\epsilon_2}{\epsilon_1} \quad (8)$$

where E_1 , E_2 , d_1 , d_2 , ϵ_1 and ϵ_2 are the electric fields, thicknesses and dielectric constants of insulator 1 and insulator 2, respectively.

From Equ. (8), the ratio of electric fields induced by external voltage in insulator 1 and insulator 2 is proportional to $\frac{\epsilon_2}{\epsilon_1}$. Assuming insulator 1 is tunneling barrier, then the higher

parameter	Model 1		Model 2	
	insulator 1	insulator 2	insulator 1	insulator 2
ϵ	high	low	low	high
d	thick	thin	thin	thick
C	small	large	small	large
E	small	large	large	small

TABLE I: The requirements for the electric properties of materials and film thickness. ϵ , d , C and E are dielectric constant, film thickness, capacitance and electric field, respectively.

dielectric constant ratio of insulator 2 to insulator 1, the higher the tunneling efficiency. Similar result can be deduced for insulator 2 as tunneling barrier. High electric field imposed on insulator 2 as in Model 1 may shorten the device lifetime due to oxide breakdown. [7]

C. Stored charge

From Eqs. (4)-(6), for Q_{fg} induced voltages, the voltage applied on insulator 1 equals to the summation of the voltage on insulator 2 and that on inverse layer, but with opposite signs. The voltage applied on the inversion layer determines the state of the transistor to be on or off. Then the higher the Q_{fg} induced voltage on inverse layer is, the higher the performance will be obtained. From Eqs. (5) and (6), Equ. (9) is deduced.

$$\frac{\partial V_3}{\partial Q_{fg}} / \frac{\partial V_2}{\partial Q_{fg}} = \frac{C_2}{C_3} \quad (9)$$

When the device is in accumulation or flat band state, no inversion layer exists. $C_3 \rightarrow \infty$. All the Q_{fg} induced voltage is applied on insulator 2. It is trivial and the transistor is off. When the device is in inversion, C_3 is finite, which is determined by the semiconducting substrate largely. According to Equ. (9), the ratio of Q_{fg} induced voltages on inverse layer and insulator 2 equals to $\frac{C_2}{C_3}$. To obtain strong inversion, the larger value of Equ. (9) is needed, which demands high value of C_2 .

D. Discussion

According to each criteria above, the requirements for materials and film thicknesses can be summarized in Table I. The contradiction discussed in Section II can be clearly seen. For Model 1, ϵ_2 is low, d_2 is thin. To obtain large C_2 , d_2 will be pushed to extreme thin. This contradiction compromises of the device performance. The situation becomes severe when the size of devices approaches extreme and cannot be conquered finally. For insulator 1, similar situation is faced. However, in Model 2, the contradiction vanishes. High ϵ , large C and thick d for insulator 2 can be satisfied at the same time. And it is the same for insulator 1.

Ferroelectric NVM is deemed as a candidate to replace the current workhorse, floating gate NVM. However, according to our analysis, this would set high requirements for the ferroelectric materials. A typical ferroelectric NVM structure is shown in Fig. 1(c), [8] which is similar to Model 2. The electric dipole moment induced by external voltage is equivalent to charge injection from top gate electrode. Then the analysis on Model 2 can also be applied. Accordingly,

Material	ϵ	bandgap (eV)	CB offset (eV)	VB offset (eV)
Si		1.1		
SiO ₂	3.9	9	3.2	4.7
HfO ₂ , doped HfO ₂	~ 25	~ 6.0	1.4	3.5
HfSiO ₄	11	6.5	2.8	3.6
Al ₂ O ₃	9	8.8	2.8	4.9
SrTiO ₃	2000	3.2	0	2.1
La ₂ O ₃	30	6	2.3	2.6
Ta ₂ O ₅	22	4.4	0.35	2.95
TiO ₂	80	3.5	0	2.4
Y ₂ O ₃	15	6	2.3	2.6
ZrO ₂	25	5.8	1.5	3.2
Si ₃ N ₄	7	5.3	2.8	1.4
a-LaAlO ₃	30	5.6	1.8	2.7

TABLE II: Properties of high-k materials. [12] The CB and VB offsets are relative to Si. The data of Si and SiO₂ are listed for comparison.

the requirements for ferroelectric NVM are the same as those in Model 2. To efficiently change the dipole moment, the higher the electric field applied on the ferroelectric film is, the better the performance. However, as we know the dielectric constant of ferroelectric materials is often very high, e.g. several thousand for Pb(Zr_xTi_{1-x})O₃ and BaTiO₃ at room temperature. This lowers the efficiency of electric field applied on it according to Section IV-B. If a high voltage is applied, the electric field in insulator 2 will be very high, which makes it easy to break down. [7] To avoid this, insulator 2 can be simply removed. However, the depolarizing electric field under direct contact of ferroelectric and semiconductor significantly decrease retention time. [9]

The proposed structure is very similar to the traditional one, so that many other technologies, which are to improve NVM performance, can be applied without difficulties, such as multi-level cell [10] and 3D stacking technology. [11]

V. MATERIAL SELECTION AND STRUCTURE GROWTH

A. Material selection

In practical devices, nanoparticle is ideal for charge storage medium, for its size suitable for small scale device fabrication. Narrow bandgap material particles, such as Si nanoparticles, are desired to use as floating gate material. SiO₂ can be used as low-k material for its excellent stability and insulation. There are many high-k materials can be selected, which have been extensively studied and are listed on Table II. [12] From Table II, it is clear that dielectric constant, bandgap, conduction band (CB) offset and valance band (VB) offset distribute widely. Because high-k material acts as gate dielectric, charge tunneling is not desired. Thus large CB/VB band offset is desired. From Table II, except SrTiO₃, Ta₂O₅ and TiO₂, the CB/VB offsets are larger than 1.4 eV for all other materials. This makes it easy to choose the fitted material to design NVM devices.

B. Feasibility of structure growth

Nowadays, film growth techniques have been developed very well. Among them, MOCVD, MBE, PLD, etc. can be chosen for their reliable high film quality and reproducibility.

The problems, which may influence the device performance, are the quality of narrow bandgap material nanoparticles inserted between high-k and low-k dielectric layers.

VI. CONCLUSIONS

In summary, we pointed out the difficulty on scaling down the device size in NVM and proposed a new structure to overcome it. By analysis, it is possible to use this structure to achieve scaling down, low power consumption, high writing speed and long retention time.

VII. POSTSCRIPT

This idea was inspired by my previous work. [13], [14]

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